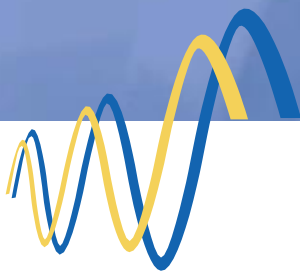
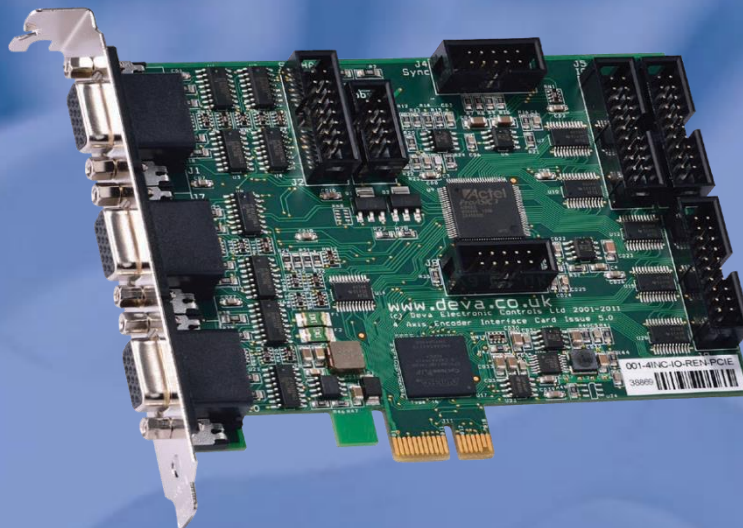


ENCODER INTERFACES

Deva001 Encoder Interface Card User's Manual



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- Overview
- Hardware Installation
- Software Installation
- Incremental Encoder Interface Hardware
- Absolute SSI Interface Hardware

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Glossary/Definition of Terms

Abbreviation/Acronym	Definition
BIOS	Basic Input/Output System
CMM	Coordinate Measuring Machine
DLL	Dynamic Link Library
DRO	Digital Readout
FIFO	First In First Out
I/O	Input/Output
LLB	LabVIEW Library
LSW	Least Significant Word
MSW	Most Significant Word
OS	Operating System
PCI	Peripheral Component Interconnect
PCle	Peripheral Component Interconnect express
SSI	Synchronous Serial Interface
TTL	Transistor-Transistor Logic
VI	Virtual Instrument
WDM	Windows Driver Model

1 Overview

1.1 About this Manual

This manual covers the Deva001 Encoder Interfaces and discusses features and potential applications. In addition, hardware and driver installation is detailed herein. For programming details, please refer to the Enclib SDK Programming Guide and/or DevaCMMCtrl SDK Programming Guide.

1.2 Deva Encoder Range Features

The Deva001 and Deva037 range of 3 and 4-axis Incremental and Absolute Encoder Interfaces are designed to enable simultaneous reading of 3 or 4 encoders per card, using a PC based system. Thus, with four 4-axis cards installed, up to 16 encoders can be supported by one system (Deva001 only). The encoders can be used for a wide range of measurement applications such as Coordinate Measuring Machines (CMMs).

For specific details of the capabilities of a particular interface, please refer to the User's Manual for that interface.

The range is provided with native drivers and additional support for Peripheral Component Interconnect express (PCIe), Peripheral Component Interconnect (PCI) and (Deva037 only) Universal Serial Bus (USB), all of which are supplied on a USB stick.

In addition to the native drivers (including Deva's proprietary Dynamic Link Library (DLL) called Enclib), the USB stick supplied with the product also contains, for CMM applications, DevaCMMCtrl, which may be installed to allow users to program and customise their machine to their specific requirements.

Enclib is the native interface should the user wish to develop bespoke software, whereas DevaCMMCtrl provide interfaces to many existing software packages. For use of DevaCMMCtrl, please refer to the DevaCMMCtrl SDK Programming Guide.

Note: DevaCMMCtrl may not be appropriate for all Deva001 applications since not all functions are supported. Please contact support@deva.co.uk for advice if necessary.

1.3 Deva001 Product Features

1.3.1 Introduction

Deva001 is available as an Incremental or Absolute Interface Card, both of which are available in PCIe and PCI variants, effectively meaning the user has four options from which to choose.

This manual details the commonalities and variations across the options and further describes the installation of Deva001 and the facilities it offers. For more detailed information regarding the use of Enclib or DevaCMMCtrl (see Section 1.2), refer to the relevant User's Manual/Programming Guide.

Note: Software support is an ongoing activity; if support for a particular application or operating system is not detailed in our documentation as provided, contact support@deva.co.uk to determine current, or future, availability.

1.3.2 PCIe features

1.3.2.1 PCIe Incremental Interface

- Four axes. Four 32-bit 40Mhz position registers
- Marker input (freeze / capture) for each encoder channel
- Renishaw probe input
- Synchronization and triggering facilities
- 48 configurable TTL I/Os
- Differential or single-ended inputs (RS422, NPN, PNP, TTL)
- 3-stage digital input filters
- +5V and +12V fused power supplies available on encoder connectors
- Timer / Event driven interrupt logic

1.3.2.2 PCIe Absolute Interface

- Four axes. Four 32-bit adjustable (2.78Mhz – 87kHz) position registers
- Programmable data and scan rates
- Programmable bit length
- Synchronization and triggering facilities
- 48 configurable I/Os
- Power fail/parity detection
- Gray and binary format support (with conversion)
- +5V and +12V fused power supplies available on encoder connectors

1.3.3 PCI features

1.3.3.1 PCI Incremental Interface

- Three axes. Three 32-bit 10Mhz position registers
- Marker input (freeze / capture) for each encoder channel
- Renishaw probe input
- Synchronization and triggering facilities
- 48 configurable TTL I/Os
- Differential or single-ended inputs (RS422, NPN, PNP, TTL)
- 3-stage digital input filters
- +5V and +12V fused power supplies available on encoder connectors
- Timer / Event driven interrupt logic
- -12V output

1.3.3.2 PCI Absolute Interface

- Three axes. Three 32-bit adjustable (2.78Mhz – 87kHz) position registers
- Programmable data and scan rates
- Programmable bit length
- Synchronization and triggering facilities
- 48 configurable I/Os
- Power fail/parity detection
- Gray and binary format support (with conversion)
- +5V and +12V fused power supplies available on encoder connectors
- Timer / Event driven interrupt logic
- -12V output

1.4 Software Support

A variety of software drivers and libraries are provided with the interface card to enable software development to be performed within several operating systems and applications. Software development is an ongoing activity, so if support for a particular application or operating system is not currently provided, please contact support@deva.co.uk to determine its availability.

1.4.1 Windows10/ Windows8/ Windows7/ WindowsXP 32/64

Both PCIe and PCI cards are supported in Windows10/ Windows8/ Windows7/ WindowsXP 32/64 by a Windows Driver Model (WDM) driver. The driver supports Deva's standard programming interface 'Enclib'. In addition, where the card is to be used in a CMM application, further programming facilities are offered by another application, 'DevaCMMCtrl'.

Please refer to the Enclib and/or DevaCMMCtrl SDK Programming Guides for more detailed information, including the capabilities of each.

1.4.2 Linux

Deva001 supports installation on a Linux OS. Please contact support@deva.co.uk if you have a requirement for this driver and/or require assistance with installation.

1.4.3 National Instruments LabVIEW

LabVIEW support is provided via a LabVIEW Library (LLB) of Virtual Instruments (VIs) which allow access to the device driver functions. These VIs allow users to develop applications very quickly using the LabVIEW system.

1.4.4 Digital Readout

A Digital Readout (DRO) displays all the common facilities of the Deva001. This enables users to quickly verify that the Deva001 is installed correctly and to make checks of the system without having to write their own software.

The DRO will handle up to four cards (12 axes) and displays both absolute and incremental positions. The DRO also displays the Marker Register, Probe Register and allows control of the probe and footswitch options.

To allow the user to read meaningful values, each axis of the DRO may be independently scaled to display real units.

For the Incremental Card all facilities, such as marker and probe, may be toggled on and off. If a probe is activated, the probed values are shown in the Probe Register whilst if a marker is activated the value is shown in the Marker Register.

For the Absolute SSI Card, it is possible to configure all features via a pop-up menu.

1.5 Typical applications

A few examples are given below to illustrate how the Deva001 may be effectively used within a target application.

1.5.1 Coordinate Measuring Machine

In this application the linear incremental encoders from the X, Y and Z axes are connected to the X, Y and Z channels of the Deva001. Each encoder has a marker or index signal which is connected to the M input which will allow a reference cycle to be performed when the equipment is switched on. A measurement probe is connected to the Renishaw touch probe input, allowing the X, Y and Z axes positions to be captured when the probe is deflected.

1.5.2 Synchronised measurement of encoders

The PCI / PCIe variants of the Deva001 can make measurements of encoder position synchronised in hardware to several different events including timer, pulse generator, axis compare and digital input. The pulse generator is programmed to generate, for example, an event every ten counts of the master encoder. The card is programmed so that every time an event is generated all encoder positions are captured. Captured data is placed in a user configurable First In First Out (FIFO) buffer and may be retrieved by user software at any time.

1.5.3 Telescope directional feedback

To measure the direction of a telescope on a turntable a single turn absolute Synchronous Serial Interface (SSI) encoder may be employed at the centre of rotation. If greater resolution is required a multi-turn encoder may be employed at the circumference of the table. An absolute SSI encoder has the advantage that the telescope position is always available and hence the telescope does not need to be rotated through 360 degrees whenever the power is re-applied.

1.6 Accessories

The Deva001 Incremental and Absolute Encoder Interfaces are supplied with three high density 15-way 'D' type connectors and matching shells for 'X', 'Y' and 'Z' encoders. For the PCIe variant, an additional ribbon cable with 15-way HD connector and PC bracket is available upon request. This provides a fourth 15-way 'D' type connector for connection of a fourth 'S' channel.

Deva can supply a wide range of cables, pre-wired and tested for use with the Deva001. Details are available on request.

2 Hardware Installation

2.1 System requirements

The interface cards require a PC computer with a minimum of one spare PCI/PCIe slot and in Windows10/ Windows8/ Window 7/ WindowsXP 32/64 operating systems. Both 32 and 64-bit operating systems are fully supported. Limited Linux support is available but is not covered in depth herein.

2.2 Hardware installation

To install a Deva001card, ensure all power to the host PC is isolated and open the PC case (usually requires removal of crosshead screws or knurled thumbscrews).

Taking appropriate anti-static precautions, locate a spare PCI or PCIe slot on the motherboard, and remove the protective cover for the associated bay on the rear of the PC. This is usually secured by a single screw but, occasionally, a 'knock-out' cover will be fitted which requires to be physically pushed out.

Position the card in the slot and secure to the bay with a single screw.

For PCIe variants, where the fourth 15-way 'D' type connector is to be installed, repeat the above steps for the extra connector/bracket and plug the ribbon cable into the 'S-CHAN' header on the card.

Ensure everything is seated and secure and close up the PC case. The PC can now be reconnected to power and booted, and driver installation can commence, as detailed in Section 3.

Deva to supply additional info re other headers on the card?

3 Software Installation

3.1 Overview

3.1.1 Interfaces

The Deva001 3 and 4-axis encoder interface cards are supplied with a software support USB stick containing support for all Deva001 encoder interfaces, along with support and information for many of Deva's other products.

The USB stick includes a number of software items which may be used with Deva001.

In addition to the native drivers (including Deva's proprietary Dynamic Link Library (DLL) called Enclib), the USB stick also contains, for CMM applications, DevaCMMCtrl, which may be installed to allow users to program and customise their machine to their specific requirements.

Enclib is the native interface should the user wish to develop bespoke software, whereas DevaCMMCtrl provide interfaces to many existing software packages.

For use of Enclib and DevaCMMCtrl, please refer to the Enclib SDK and/or DevaCMMCtrl SDK Programming Guides.

Note: DevaCMMCtrl may not be appropriate for all Deva001 applications since not all functions are supported. Please contact support@deva.co.uk for advice if necessary.

3.1.2 Windows10/ Windows8/ Windows7/ WindowsXP 32/64

To install Deva001 on a Windows OS, refer to Section 3.2.

3.1.3 Linux

Deva001 supports installation on a Linux OS. Please contact support@deva.co.uk if you have a requirement for this driver and/or require assistance with installation.

3.1.4 MS-DOS

The MS-DOS driver has been discontinued. Please contact support@deva.co.uk if you have a requirement for this driver and/or require assistance with installation.

3.2 Windows10/ Windows8/ Windows7/ XP 32/64

Depending on the version of Windows in use, driver installation varies slightly. The following text is therefore generic. In case of difficulty, consult the help files for your OS or contact support@deva.co.uk.

3.2.1 Native drivers (including Enclib)

Important: If intending to use DevaCMMCtrl, do **not** follow these instructions as driver conflicts may result. Instead, proceed straight to Section 3.2.2 below.

Once the card has been installed (Section 2.2), re-boot the system and Windows will indicate that a new device has been found. Navigate to the Windows Device Manager and the card will usually be shown as 'Unknown Device' or 'Encoder Interface'.

In Device Manager, double-click, or right-click, the appropriate device (ie 'Unknown Device' or 'Encoder Interface'). Windows will give the option to 'Install Driver' or 'Update Driver', again depending on OS.

Ensure the Deva supplied USB stick is plugged into a USB socket on the PC and select the 'Install Driver' or 'Update Driver' button. When prompted, browse to the USB stick and locate the folder 'X:\Gold CD Relxx' ('X' will vary according to the PC setup and Deva software release).

Click on 'Install' or 'OK' and follow the ensuing instructions to complete the installation. Windows will locate the correct drivers for your card and will indicate when they have been successfully installed.

3.2.1.1 Testing

Ensure that at least one compatible encoder is plugged into a 15-way 'D' type connector on the card (in the case of the following example, an encoder is connected to the X Axis). See Sections 4.1 and 5.1.

The installation may then be tested using the supplied DRO program, which can be found on the USB stick at 'X:\Gold CD Relxx\PC interface products\Deva001\Issue x.x\Windows\utils\Win32' ('X' and 'x' will vary according to Deva software release and the PC setup. A Win64 variant is also available for 64-bit systems, if preferred).

Open the DRO program and a display similar to Figure 3.1 will be seen.

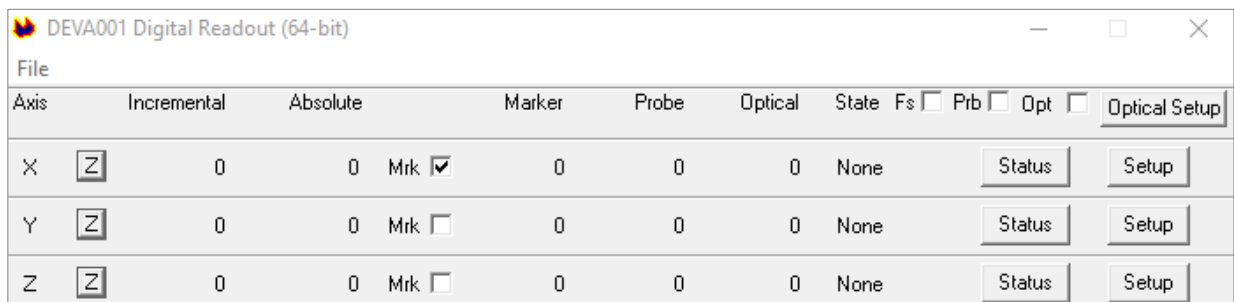


Figure 3.1 DRO Display 'at rest'

Manually move the encoder (or press the probe if a probe has been connected). Depending on the card installed, either the Incremental or Absolute reading should change to indicate a displacement as shown in Figure 3.2. This indicates that both hardware and software have been installed successfully.

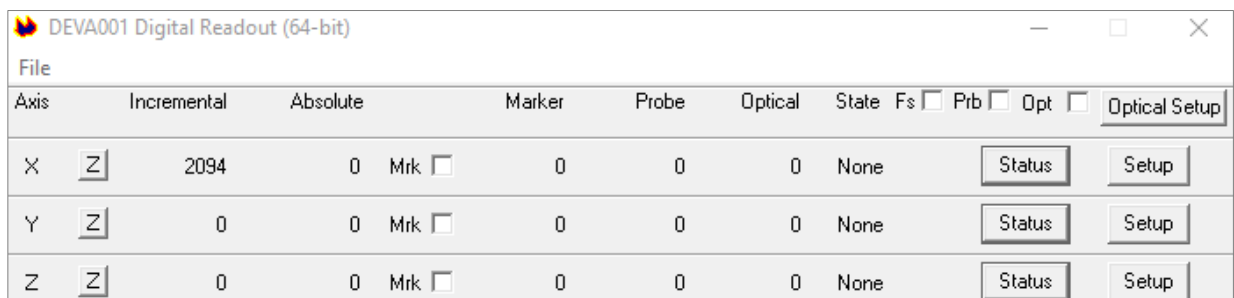


Figure 3.2 DRO Display after encoder displacement

3.2.2 DevaCMMCtrl drivers and software

Important: If native drivers have previously been installed, they must be uninstalled before DevaCMMCtrl installation or driver conflicts may result. If required, guidance on driver removal will be found in the help files of the OS.

Once the card has been installed (Section 2.2), re-boot the system and Windows will indicate that a new device has been found. Navigate to the Windows Device Manager and the card will usually be shown as 'Unknown Device' or 'Encoder Interface'.

In Device Manager. Double click, or right click, the 'Unknown Device' or 'Encoder Interface'; Windows will give the option to 'Install Driver' or 'Update Driver', again depending on OS.

Ensure the Deva supplied USB stick is plugged into a USB socket on the PC and select the 'Install Driver' or 'Update Driver' button. When prompted, browse to the USB stick and locate the folder 'X:\Deva CMM Control Relxx' ('X' will vary according to the PC setup and Deva software release).

Click on 'Install' or 'OK' and follow the ensuing instructions to complete the installation. Windows will locate the correct drivers for the card and will indicate when they have been successfully installed.

3.2.2.1 Utility software installation and configuration

In order to configure Deva001 with DevaCMMCtrl, it is necessary to install the Deva Tools utility, as follows:

With the USB stick plugged into the host PC, browse to 'X:\Deva CMM Control Relxx\DevaCMMCtrl\Deva Tools\Setup Deva Tools' ('X' will vary according to the PC setup) and click 'Next' or 'Install'. Follow the instructions to complete installation.

The first step on a new installation, after installing Deva Tools, is to use the Deva Config Editor to install a default configuration for the card. This is performed by opening the Deva Config Editor, when a display similar to Figure 3.3 will be seen.

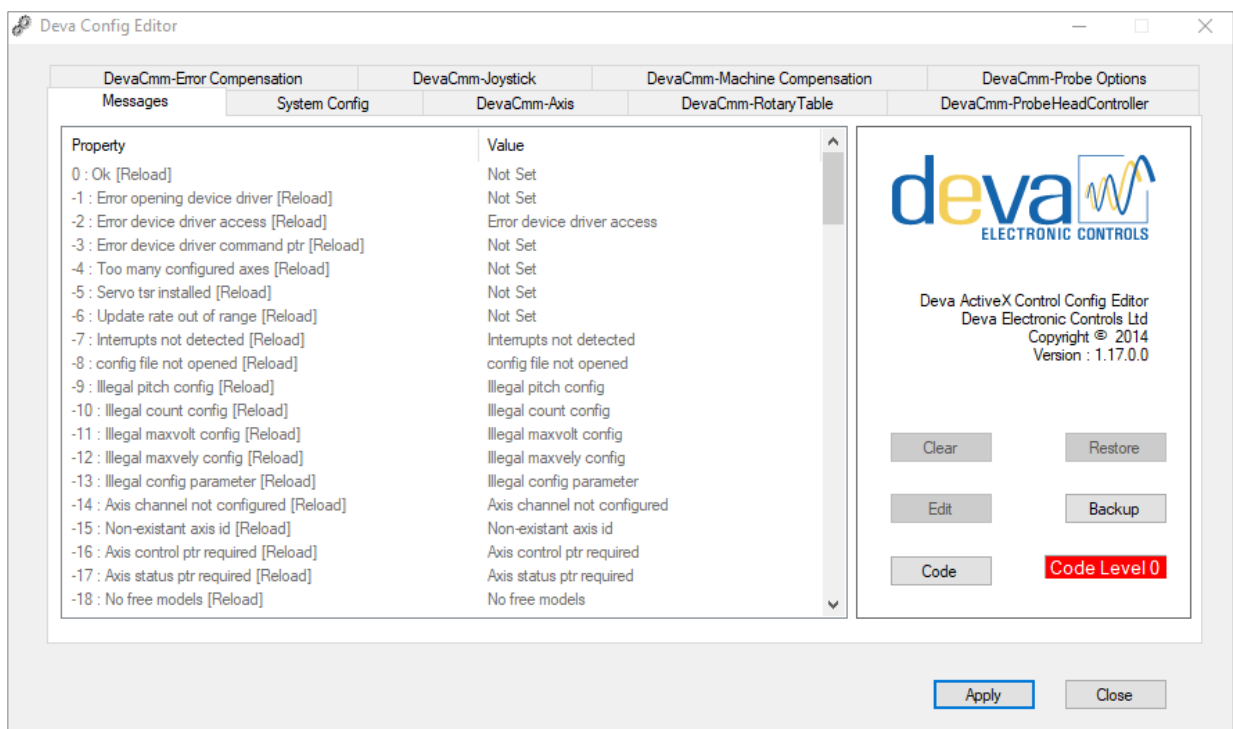
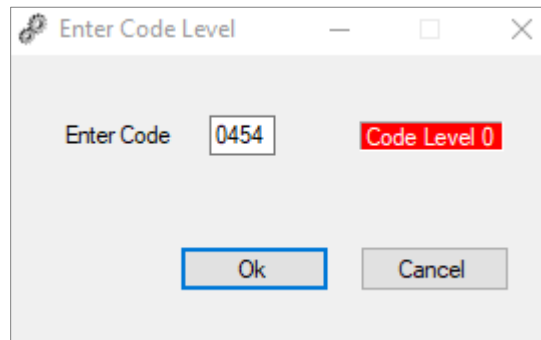


Figure 3.3 Config Editor – initial screen

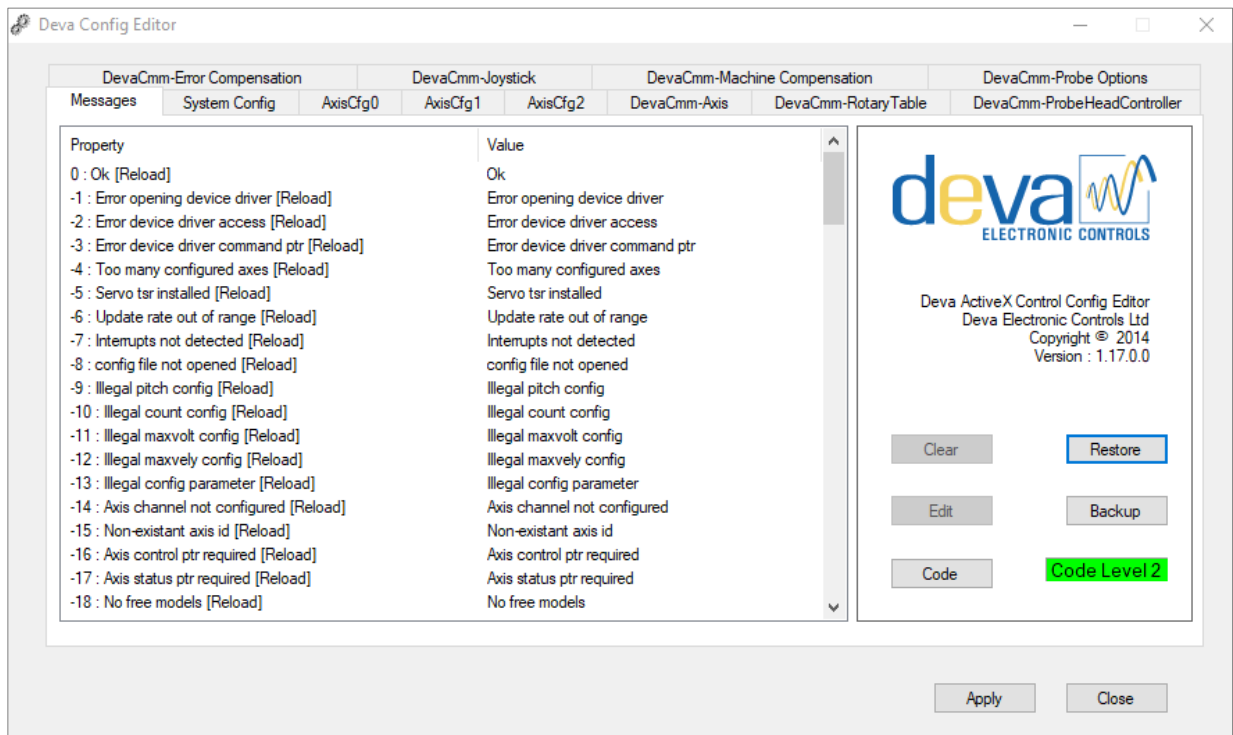
Press the 'Code' button and, on the pop-up displayed, enter the code 0454 in the code dialog, as shown in Figure 3.4 below. Press 'Ok'. The main panel will change to a display similar to Figure 3.5.

**Figure 3.4 Config Editor – code entry**

The screen will revert to the previous display (Figure 3.3) but with 'Code Level 2' displayed on a green background. Press 'Restore' and browse through the USB stick to 'X:\Deva CMM Control Relxx\DevaCMMCtrl\DefaultConfigs\Deva001CmmDefaultConfig'.

Press 'Apply', and 'Close'.

This will result in a basic configuration being set up with default values, such as number of axes and axis types as shown in Figure 3.5; the Deva Config Editor can then be used to customize the configuration as part of the machine installation. For more information see the Deva Config Editor manual.

**Figure 3.5 Config Editor – configuration enabled**

3.2.2.2 Testing

The installation may be tested using the supplied DevaCMM Control Panel.

Ensure that at least one compatible encoder is plugged into a 15-way 'D' type connector on the card (in the case of the following example, an encoder is connected to the X Axis). See Sections 4.1 and 5.1.

Open the DevaCMM Control Panel program and a display similar to Figure 3.6 will be seen. Note that for the example shown, the X axis is datummed at Position 550.00 and the 'At Target' box is checked.

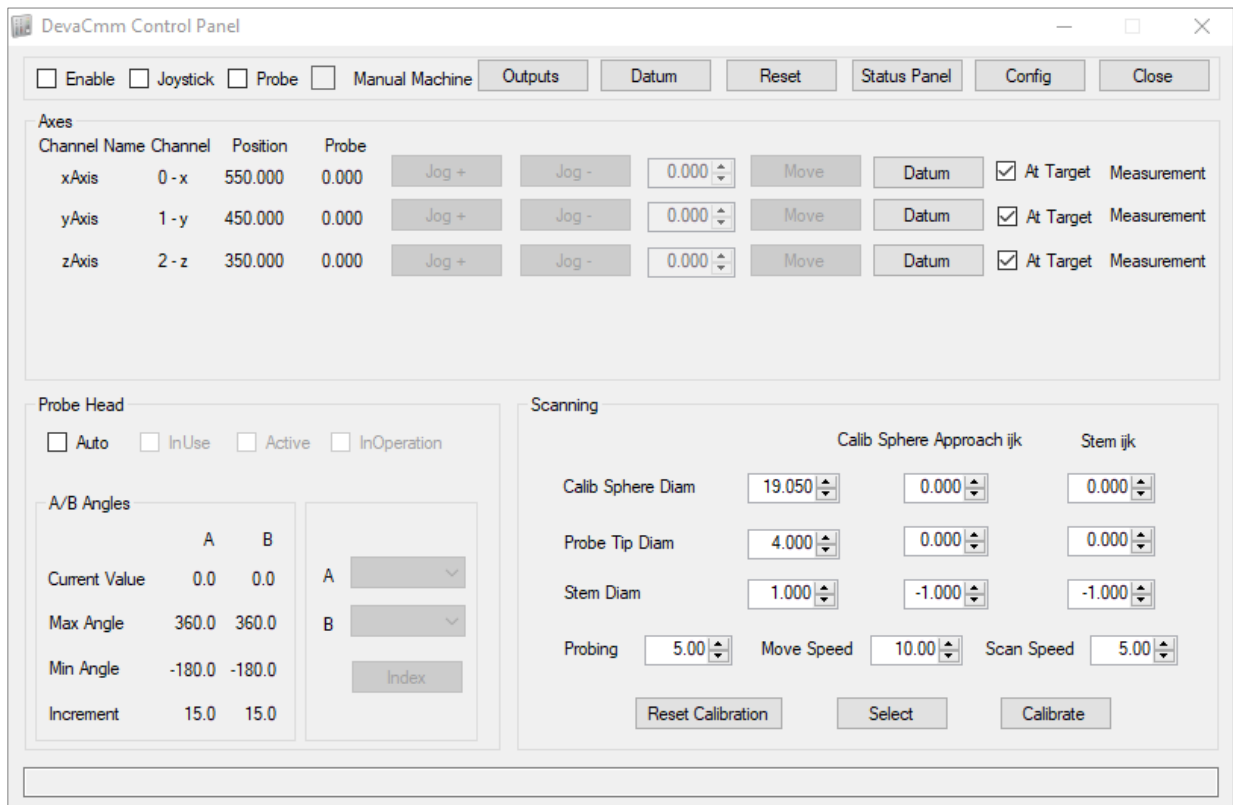


Figure 3.6 DevaCMM Control Panel Display 'at rest'

Manually move the encoder (or press the probe if a probe has been connected). The reading should change to indicate displacement as shown in Figure 3.7. In the case of the example shown, the X axis position has changed to 543.575 and the 'At Target' box is unchecked. This indicates that both hardware and software have been installed successfully.

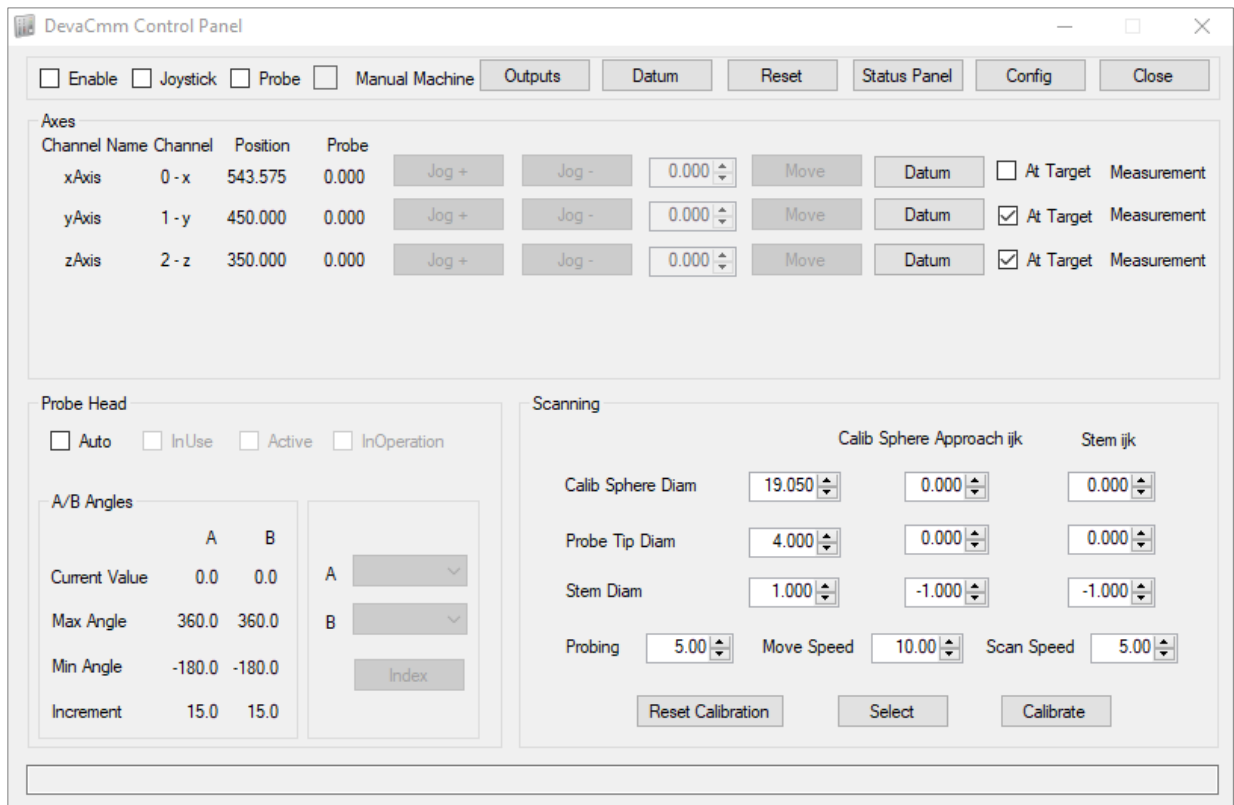


Figure 3.7 DevaCMM Control Panel Display after encoder displacement

4 Incremental encoder interface hardware

4.1 Connection details

The Deva001 has three input channels for quadrature signals from incremental encoders, designated X, Y & Z. Connection of each channel to the outside world is made through a 15-way HD-type connector. The designation of the connectors is shown in Figure 4.1.

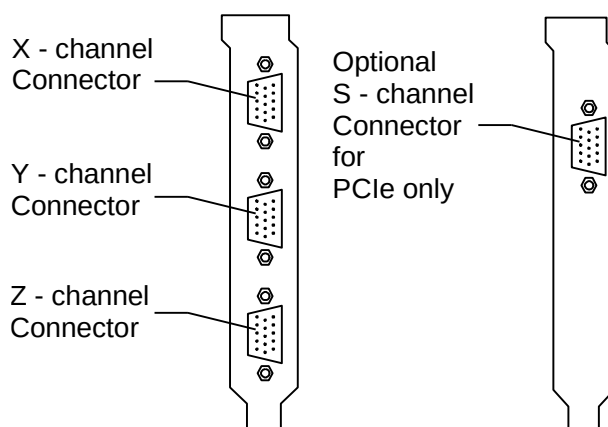


Figure 4.1 External Connections

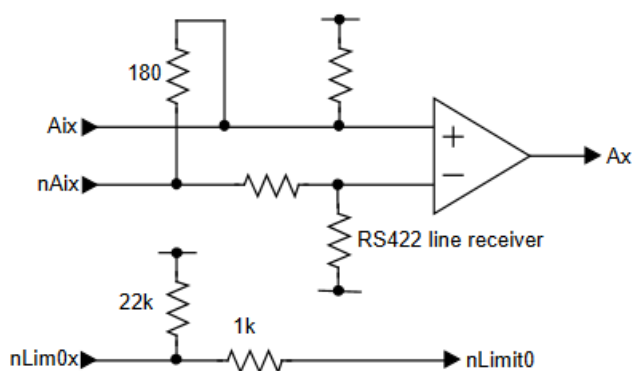
The PCIe card has an additional 4th channel. This is available on the 16-pin header labelled "S - CHAN". An additional ribbon cable with 15-way HD connector and PC bracket, as shown in Figure 4.1, is available upon request.

4.1.1 Encoder input connections

Connections to these sockets should be made with reference to the following pin-out table and simplified input circuit.

Pin Number	Signal	Function
1	Ai	A phase input
2	Bi	B phase input
3	Zi	Zero input
4	Mi	Marker input
5	nLim0	nLimit 0
6	nAi	nA phase input
7	nBi	nB phase input
8	nZi	nZero input
9	nMi	NMarker input
10	nLim1	nLimit 1
11	+12V	+12 volts supply
12	+5V	+5 volts supply
13	0V	0 volt common
14		
15	-12V	-12 volt supply*

*PCI only.



Caution: Do not connect the 15-way D-type plug of a VGA monitor into any of the encoder input channels, as damage may result.

4.1.2 Input signal descriptions

The Ai & nAi, Bi & nBi inputs are differential pairs for connection to the A-phase and B-phase quadrature outputs of an incremental encoder.

The Mi & nMi inputs are differential inputs for the channel marker signal. This function will latch the counter reading for the relevant channel, allowing an accurate reading of the position of a moving encoder to be made at a specific instant. The marker function does not stop the counter itself, which is able to continue reading the encoder position and so it will not cause the card to lose track of the system's datum position.

The Zi & nZi may be used as an alternative to the Mi & nMi inputs. In this case the driver will zero the counter readings in software.

The inputs nLim0 and nLim1 are digital inputs intended to be used to connect normally closed overtravel inputs.

The differential inputs use RS422 levels which accept 0V for logic low, and +5V to +12V for logic high. Because they are differential inputs, one input should be low when the other is high. For example, to trigger the marker function, set Mi input to high, and set nMi input to low. To turn the marker function off, reverse these logic levels.

An internal resistor network is provided which allows connection of single ended signals to the non-inverting inputs.

The +/- 12V and +5V power supply pins may be used to supply the dc power requirements for the encoders.

Note: -12V is not available from the PCIe variant.

4.1.3 Renishaw probe input connections

The Renishaw connection kit provides a 9-way female 'D' connector which may be used with the bracket supplied or mounted in a free cut-out on the PC case. Connections to this socket should be made with reference to the following pin-out table.

Pin Number	Signal	Function
1	LED C	LED cathode
2	0V	(0V)
3	LED A	LED anode
4	Probe +	Probe
5	Probe -	Probe 0V
6	Siren +	Siren +5V
7	Siren -	Siren 0V
8	FootSw +	Footswitch input
9	FootSw -	Footswitch 0V

4.1.4 Digital I/O connections

There are three 20 pin headers labelled IO0, IO1 and IO2 which provide access to three groups of 16 bits of digital I/O. The I/O conforms to 5V TTL levels; Voh minimum 2.4V at -8mA and Vil maximum 0.4V at 12mA.

4.1.4.1 Digital I/O connector 0 connections

The direction of I/O connector 0 pins is fixed. Pins 1 to 8 (IO0 to IO7) are outputs. Pins 9 to 16 (IO8 to IO15) are inputs.

Pin	Connector IO0	Special Function
1	IO0 / UR0 / MOx / AC00x	User request 0 / Marker occur x / Axis compare 0 occur
2	IO1 / UR0 / MOy	User request 0 / Marker occur y
3	IO2 / UR0 / MOz	User request 0 / Marker occur z
4	IO3 / UR0 / MOs	User request 0 / Marker occur s
5	IO4 / PO / FO / UR0	Probe occur / Footswitch occur / User request 0
6	IO5 / TMRO / TMRTCNT / UR0	Timer occur / Timer terminal count / User request 0
7	IO6 / PG00 / PG0TCNT / UR0	Pulse gen. 0 occur / Pulse gen. 0 terminal count / User request 0
8	IO7 / - / - / UR0	User request 0
9	IO8 / CDI0x	Channel X digital input 0
10	IO9 / CDI0y	Channel Y digital input 0
11	IO10 / CDI0z	Channel Z digital input 0
12	IO11 / CDI0s	Channel S digital input 0
13	IO12 / BDI0	Board digital input 0
14	IO13	
15	IO14	
16	IO15	
17	GND	
18	GND	
19	+5V	
20	+12V	

4.1.4.2 Digital I/O connectors 1 and 2 connections

The direction of I/O connectors 1 and 2 pins is software-configurable in groups of 8 (1 to 8 and 9 to 16).

Pin	Connector IO1	Connector IO2
1	IO16	IO32
2	IO17	IO33
3	IO18	IO34
4	IO19	IO35
5	IO20	IO36
6	IO21	IO37
7	IO22	IO38
8	IO23	IO39
9	IO24	IO40
10	IO25	IO41
11	IO26	IO42
12	IO27	IO43
13	IO28	IO44
14	IO29	IO45
15	IO30	IO46
16	IO31	IO47
17	GND	GND
18	GND	GND
19	+5V	+5V

Pin	Connector IO1	Connector IO2
20	+12V	+12V

4.1.5 Sync connector

The sync connector provides a method of linking cards in hardware to allow events to be routed from one card to another. In general, a ribbon cable connecting all 10 connections between all cards is required.

Pin Number	Function
1	Sync0 (Timer occur)
2	GND
3	Sync1 (Pulse Generator 0 occur)
4	GND
5	Sync2 (Axis Compare 0 occur)
6	GND
7	Sync3 (Axis Compare 1 occur)
8	GND
9	GND
10	GND

4.2 Functional description

The Deva001 is designed to interface up to three (PCI) or four (PCIe) incremental encoders or linear scales to the PCI/PCIE bus. The following sections describe the various functions of the interface; for detailed description of how to program these facilities please refer to Section 4.3.

4.2.1 Quadrature input

Each encoder channel has four differential / single ended input circuits designated A, B, Z and M. The A and B inputs accept the quadrature signals from the encoder and drive an up/down counter via a x4 directional discriminator circuit. The counter has 32-bit resolution and may be read at any time. The maximum count rate is in excess of 10MHz.

4.2.2 Marker input

The M input circuit designated marker is a positive edge triggered input which can synchronously latch the counter value. To gain the most accurate result the input conditioning circuit latches the counter when both A and B inputs are at a logic 1 level. The user must therefore phase the A and B signals carefully to meet this criterion. Should this not be achievable, circuit operation is still possible, although the latched value will not be accurate to a single count. Correct phasing may also be achieved by using the input inverters on signals A, B and M.

To use the marker input, the marker circuit must be enabled. Once a positive edge has occurred on the marker input, the counter is latched when both A and B are at logic '1'. The marker latch register may now be read while the counter continues to maintain position. To enable the marker latch to capture a further event the marker function should be disabled and then re-enabled. Marker synchronisation with signals A and B can optionally be disabled.

4.2.3 Zero input

The Z input circuit designated zero is a positive edge triggered input which can asynchronously latch the counter value. It has been provided to maintain compatibility with previous issues and offer more flexibility when connecting encoders. The marker function, which accurately latches the counter value, is equally suited to performing a zero-type operation by using the latched value as an offset, which is subsequently subtracted from the counter reading.

4.2.4 Renishaw Probe Interface

The Deva001 incorporates a Renishaw compatible probe input. This input provides the correct signal conditioning to allow a volt-free, contact type touch probe to be used. The probe function works like the marker function but latches all three axis counters simultaneously. Unlike the marker function, it operates asynchronously and hence does not require that the A and B signals are at a logic '1' level. The probe function has its own enable bit.

The card also incorporates an output to drive the probe LED, an output to drive an audible sounder, and a further input to allow the probe to be controlled via a footswitch.

4.2.5 Digital I/O

The Deva001 has 48 digital I/O lines arranged in 3 groups of 16 bits. The first group of 16 bits may be associated with special input and output functions specific to other features of the card and has hardwired directions. The direction of the other two groups may be programmed in blocks of 8 bits.

4.2.6 Pulse Generator

The Deva001 has a 16-bit Pulse Generator circuit which can produce a pulse every 'n' counts of the X axis encoder, where 'n' is programmable from 1 to 65536. The pulse can be sent directly to a digital output, cause a hardware event, or generate an interrupt. Refer to Figure 4.2 for details of which actions can be triggered by the pulse generator event.

The pulse generator range of operation (start and stop positions) may optionally be controlled through hardware. If hardware control is selected the axis compare functions are used as start and stop positions. Please note that the pulse generator function needs to be enabled for this feature to operate.

The pulse generator has both uni-directional and bi-directional modes, configurable direction when in uni-directional mode, and incorporates an optional de-glitch circuit that prevents a pulse being generated at the same position sequentially.

4.2.7 Axis Compare

The X axis has two Axis Compare registers which may be used to generate events when the axis position matches the compare position. The Axis Compare registers are shared with the Marker and Probe latches.

4.2.8 Timer

The timer is an 8-bit interval timer which can be programmed in steps of 0.1ms up to a maximum of 25.6ms. This timer may be used to generate interrupts, latch encoder positions, or trigger a digital output for external circuitry synchronisation.

4.2.9 Time Stamper

The Time Stamper is a 16-bit high speed timer with a resolution of 1 μ s. It can be programmed to latch its value on an event to provide an accurate time stamp of precisely when the event occurred.

4.2.10 Event System

Many features of the card produce events. When an event occurs, a flag called the Occur Flag is set. The Occur Flag may be polled by the user to establish that the event has occurred.

The card has a variety of actions which may be configured to respond to events. The actions include latching the current position in one of three latches, generating an interrupt, triggering a digital output, or latching a time stamp of the event.

Figure 4.2 and Figure 4.3 show the board level and channel level events, and actions which may be programmed.

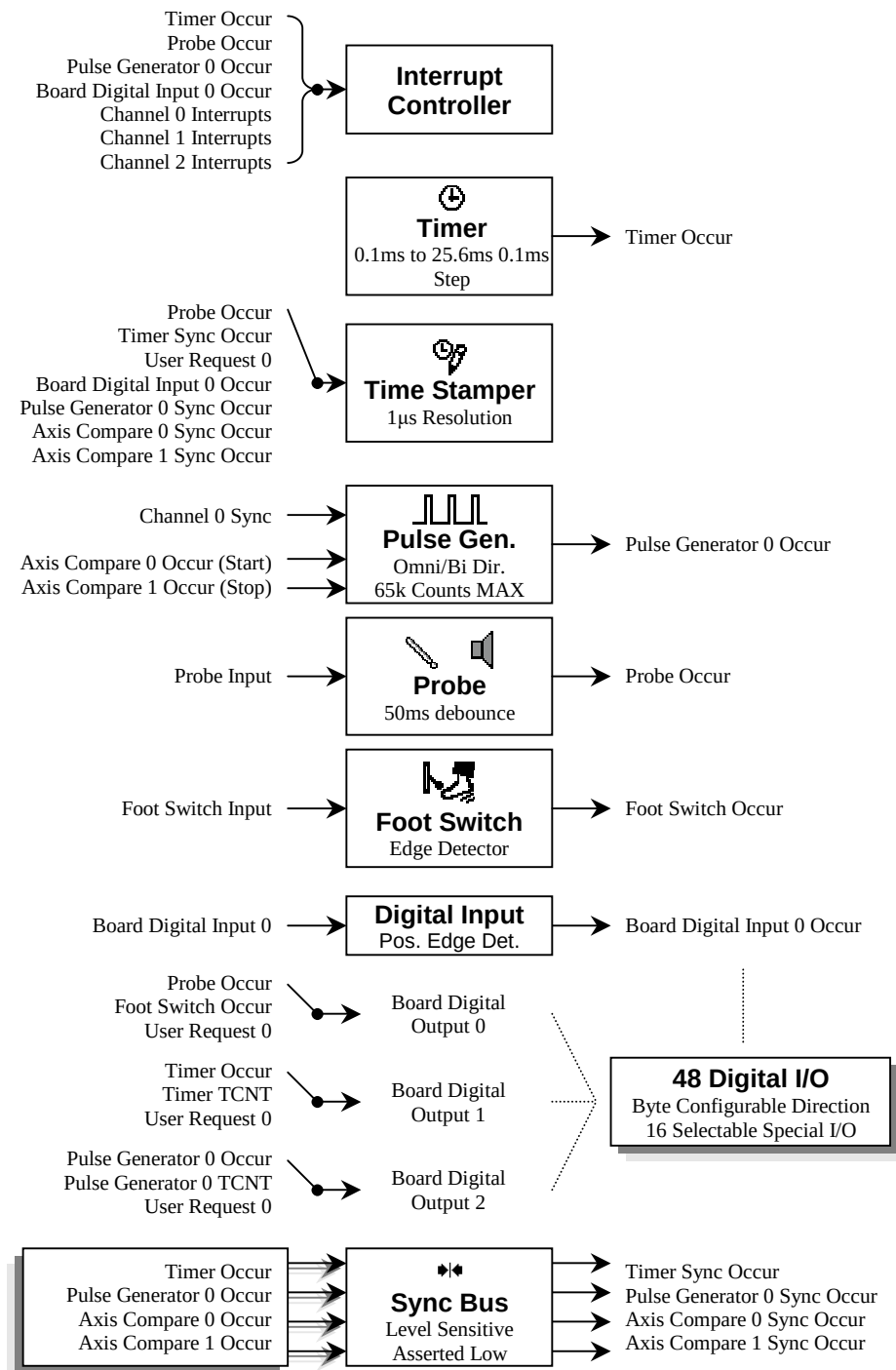


Figure 4.2 Incremental Board Level Block Diagram

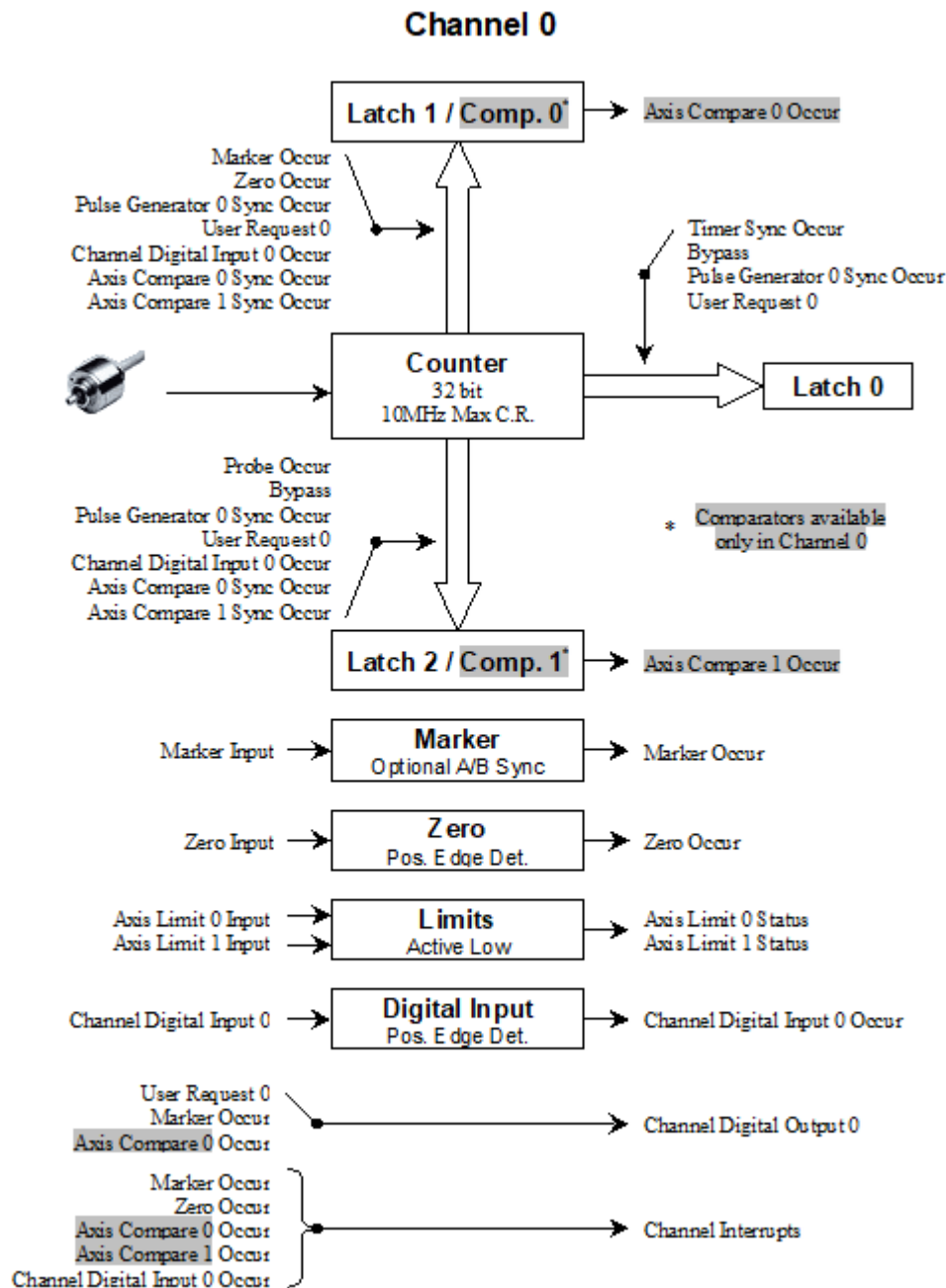


Figure 4.3 Incremental Channel Level Block Diagram

4.3 Direct hardware programming

The Deva001 incremental encoder interface card is supplied with a variety of device drivers for Microsoft Windows operating systems which perform all low-level access functions required for its operation. Using a device driver offers several benefits including the ability to re-use application software and routines with any of Deva Electronics compatible products. For applications where hardware access is essential, Appendix A gives an overview of the register set and card functionality.

5 Absolute SSI interface hardware

5.1 Connection details

The Deva001 has three input channels for SSI data signals from absolute encoders, designated X, Y & Z. Connection of each channel is made through a 15-way D-type connector. The designation of the connectors is shown in Figure 5.1.

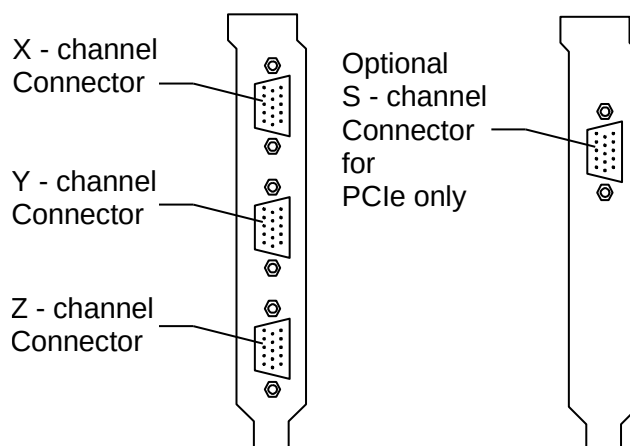


Figure 5.1 External Connections

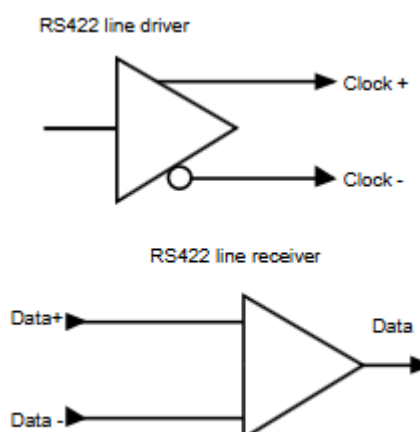
The PCIe card has an additional fourth channel. This is available on the 16-pin header labelled "S-CHAN". An additional ribbon cable with 15-way HD connector and PC bracket, as shown in Figure 5.1, is available upon request.

5.1.1 Encoder input connections

Connections to these sockets should be made with reference to the following pin-out table and simplified circuit shown.

Pin Number	Signal	Function
1	Clock+	Clock+ output
2	Out+	Out+ output
3	Data+	Data+ input
4	Spare+	Spare+ output
5		
6	Clock-	Clock- output
7	Out-	Out- output
8	Data-	Data- input
9	Spare-	Spare- output
10		
11	+12V	+12 volt supply
12	+5V	+5 volt supply
13	0V	0 volt common
14		
15	-12V	-12 volt supply*

*PCI only.



Caution: Do not connect the 15-way D-type plug of a VGA monitor into any of the encoder input channels, as damage may result.

5.1.2 SSI signal descriptions

The SSI interface uses two differential signals clock and data which have the connections **Clock+**, **Clock-**, **Data+** and **Data-**.

The Deva001 has a third uncommitted signal designated **Out** with the connections **Out+** and **Out-** which may be used to select encoder dependent features such as forward/reverse. The **Spare+** and **Spare-** connections should be left unconnected.

The Deva001 interrogates the encoder for its positional value by sending a pulse train from its clock output. The number of clock pulses depends on the bit length of the encoder.

The first high-low transition at point 1 triggers the encoder's monostable and parallel data is stored in the encoder's parallel to serial converter. While the monostable is at logic 0, no more parallel data can be stored in the parallel to serial converter.

At the first low-high transition at point 2 the most significant data bit is output by the encoder and received on the data input.

At each subsequent low-high transition in the pulse train, the next highest bit is transmitted. The pulses continuously re-trigger the monostable so that its output stays at logic 0, preventing further storage of data. When the least significant bit is received by the Deva001, the pulse train is terminated. The monostable is no longer triggered and at point 4 after an interval "tm" the output returns to logic 1, allowing the storage of new parallel data in the parallel to serial converter.

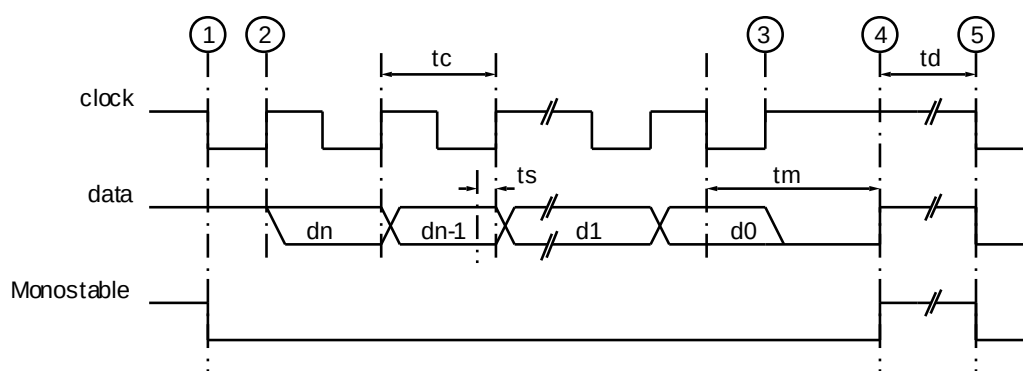


Figure 5.2 SSI Interface Timing Diagram

Register value	Clock frequency	Clock period (tc)	Setup time (ts)
0	2.78 MHz	0.36 μ s	0.1 μ s
1	1.39 MHz	0.72 μ s	0.1 μ s
2	926 kHz	1.08 μ s	0.1 μ s
3	694 kHz	1.44 μ s	0.1 μ s
4	463 kHz	2.16 μ s	0.1 μ s
5	347 kHz	2.88 μ s	0.1 μ s
6	174 kHz	5.76 μ s	0.1 μ s
7	86.8 kHz	11.5 μ s	0.1 μ s

Under normal circumstances the encoder data should go to logic 0 after point 3, returning to logic 1 at point 4 indicating the encoder is ready to be read again. The Deva001 waits for the data to return to logic 1 before it starts any subsequent readings.

If the data does not go to logic 0 at point 3 the Deva001 assumes that synchronisation with the encoder has been lost at some time before or during the reading. The Deva001 now outputs up-to 32 clock pulses until a logic 0 is detected, at this point the clock is stopped and the Deva001 waits for the encoder monostable to time out.

This re-synchronisation process makes possible the continuous mode of operation which starts a new reading as soon as the encoder indicates it is ready, without the side effect that could otherwise cause the system to lock up in an un-synchronised state in the presence of noise.

The +/-12V and +5V power supply pins may be used to supply the dc power requirements for the encoders. A -12V supply is not available from the PCIe variant.

5.1.3 Digital I/O connections

There are three 20 pin headers labelled IO0, IO1 and IO2 which provide access to 3 groups of 16 bits of digital I/O. The I/O conforms to 5V TTL levels, Voh min 2.4V at -8mA and Vil maximum 0.4V at 12mA.

5.1.3.1 Digital I/O connector 0 connections

Pin	Connector IO0	Special Function
1	IO0 / UR0 / RTRIGx / RCOx	User request 0 / Read trigger x / Read complete occur x
2	IO1 / UR0 / RTRIGy / RCOy	User request 0 / Read trigger y / Read complete occur y
3	IO2 / UR0 / RTRIGz / RCOz	User request 0 / Read trigger z / Read complete occur z
4	IO3 / UR0 / RTRIGs / RCOs	User request 0 / Read trigger s / Read complete occur s
5	IO4 / UR0	User request 0
6	IO5 / TMRO / TMRTCNT / UR0	Timer occur / Timer terminal count / User request 0
7	IO6 / - / - / UR0	User request 0
8	IO7 / - / - / UR0	User request 0
9	IO8 / CDI0x	Channel x digital input 0
10	IO9 / CDI0y	Channel y digital input 0
11	IO10 / CDI0z	Channel z digital input 0
12	IO11 / CDI0s	Channel s digital input 0
13	IO12 / BDI0	Board digital input 0
14	IO13	
15	IO14	
16	IO15	
17	GND	
18	GND	
19	+5v	
20	+12V	

5.1.3.2 Digital I/O connectors 1 and 2 connections

Pin	Connector IO1	Connector IO2
1	IO16	IO32
2	IO17	IO33
3	IO18	IO34

Pin	Connector IO1	Connector IO2
4	I019	I035
5	I020	I036
6	I021	I037
7	I022	I038
8	I023	I039
9	I024	I040
10	I025	I041
11	I026	I042
12	I027	I043
13	I028	I044
14	I029	I045
15	I030	I046
16	I031	I047
17	GND	GND
18	GND	GND
19	+5V	+5V
20	+12V	+12V

5.1.4 Sync connector

The sync connector provides a method of linking cards in hardware to allow events to be routed from one card to another. In general, a ribbon cable connecting all 10 connections between all cards is required.

Pin Number	Function
1	Sync0 (Timer occur)
2	GND
3	Sync1 (Undefined)
4	GND
5	Sync2 (Undefined)
6	GND
7	Sync3 (Undefined)
8	GND
9	GND
10	GND

5.2 Functional description

The Deva001 is designed to interface up to three (PCI) or four (PCIe) absolute SSI encoders or linear scales to the PC PCI/PCIe bus. The following sections describe the various functions of the interface, for a detailed description of how to program these facilities please refer to Section **Error! Reference source not found.**

5.2.1 Programmable clock frequency, bit length and offset

The clock frequency and encoder bit length may be independently programmed for each encoder. The frequency may be set to one of eight values in the range 78 kHz to 2.5 MHz (see Section 5.1.2 for details). The bit length may be programmed in the range 1 to 32 bits. The time taken to make a reading will depend on both the clock frequency and the bit length as follows:

Reading time = (bit length + 2) / (Clock frequency)

Bit length	Clock frequency	Reading time
12	625 kHz	22.4µs
13	625 kHz	24µs
21	2.5 MHz	9.2µs

The offset feature allows the data read from the encoder to be shifted left a further 0-15 bits. This is typically used to align the angular part of the encoder data to the 16-bit boundary. In this case the Most Significant Word (MSW) represents the number of turns and the Least Significant Word (LSW) represents the angular component.

Consider a system which has the following three encoders :

- i 15 bit single turn encoder
- ii 12 bit single turn encoder
- iii 21 bit multi-turn encoder with 13 bits of angular resolution

By applying offsets of 1, 4 and 3 bits respectively the angular component of the measurement will be aligned to the LSW of the latch in each case. As a result, all three encoders will return the same value for the same angle.

5.2.2 Power fail and parity detection

The Deva001 can be programmed to read an additional bit after the last data bit. This bit may be treated as a parity bit or a power fail bit by the Deva001. In the case of parity, the Deva001 performs a parity check and sets a status bit if the data fails the test. In the case of power failure, the extra bit is latched and may be read from the status register. These features may be independently selected for each channel.

5.2.3 Gray to binary conversion

The Deva001 can perform Gray to binary conversion on incoming encoder data in hardware. This feature may be independently selected for each channel.

5.2.4 Programmable interval timer

The Deva001 has an 8-bit interval timer which can be programmed in steps of 0.1ms up to a maximum of 25.6ms. This timer may be used to generate interrupts or start encoder readings.

5.2.5 Time Stamper

The time stamper is a 16-bit high speed timer with a resolution of 1µs. It can be programmed to latch its value on an event so to provide an accurate time stamp of when the event occurred.

5.2.6 Digital I/O

The Deva001 has 48 digital I/O lines arranged in three groups of 16 bits. The first group of 16 bits may be associated with special input and output functions specific to other features of the card and has hardwired directions. The direction of the other two groups may be programmed in blocks of 8 bits.

5.2.7 Event System

Many features of the card produce events. When an event occurs, a flag called the occur flag is set. The occur flag may be polled by the user to establish that the event has occurred.

The card has a variety of actions which may be configured to respond to events. The actions include triggering an encoder position read, generating an interrupt, triggering a digital output or latching a time stamp of the event.

Figure 5.3 and Figure 5.4 show the board level and channel level events and actions which may be programmed.

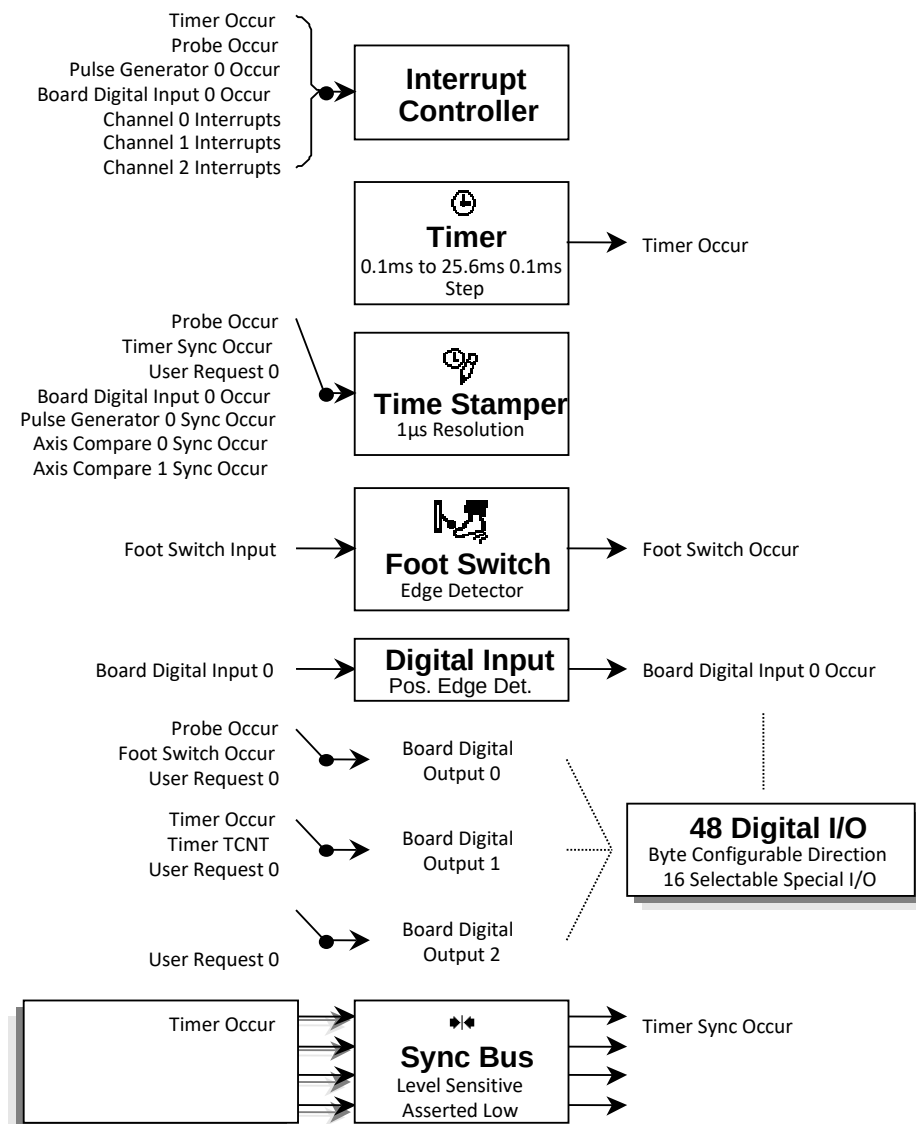


Figure 5.3 SSI Board Level Block Diagram

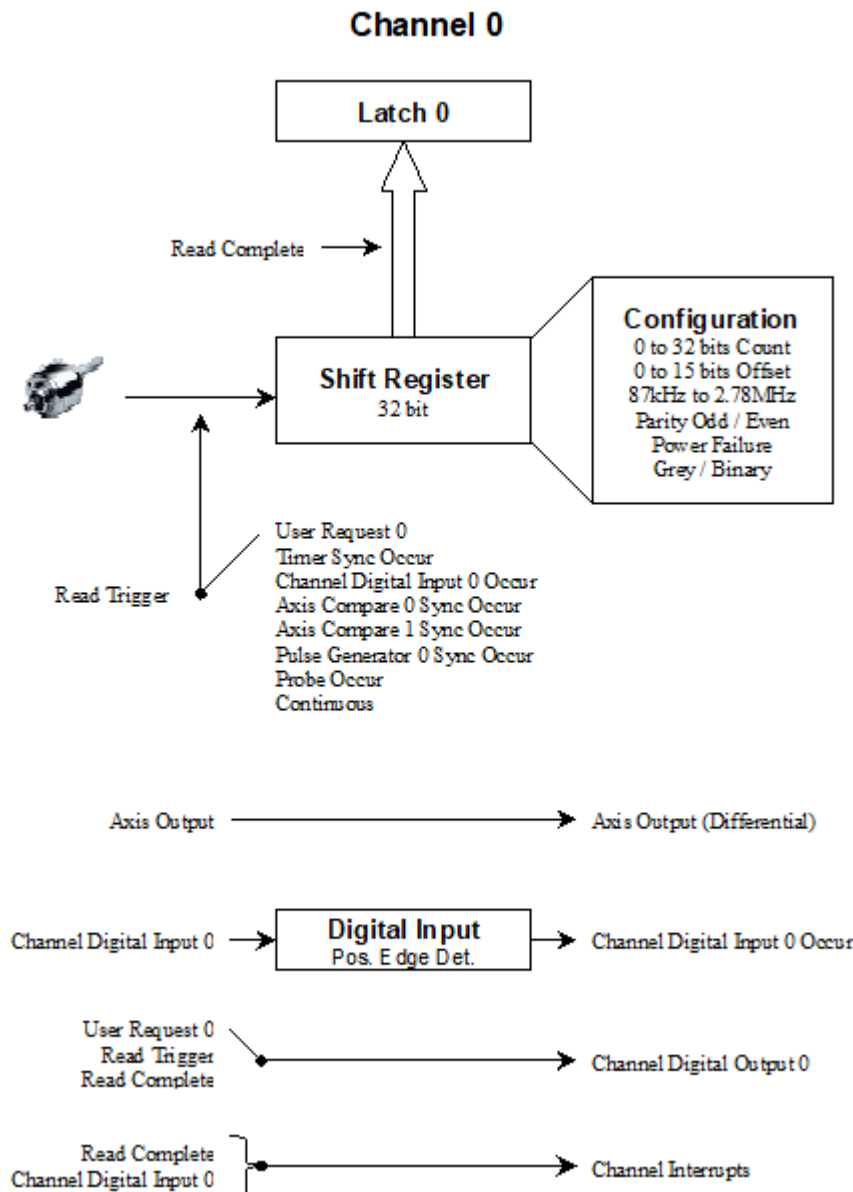


Figure 5.4 SSI Channel Level Block Diagram

5.3 Direct hardware programming

The Deva001 absolute encoder interface card is supplied with a variety of device drivers for Microsoft Windows operating systems which perform all low-level access functions required for its operation. Using a device driver offers several benefits including the ability to re-use application software and routines with any of Deva Electronics compatible products. For applications where hardware access is essential, Appendix B gives an overview of the register set and card functionality.

Appendix A - Incremental Card Register Reference

The Deva001 Incremental Encoder Interface card is supplied with a variety of device drivers for Microsoft Windows operating systems which perform all low-level access functions required for its operation. Using a device driver offers several benefits including the ability to re-use application software and routines with any of Deva Electronics compatible products. The device drivers and the common software interface are described in Section 1 and Section 2 of this manual. For applications where hardware access is essential, the following text gives an overview of the register set and card functionality.

Register address map

The card implements several 32-bit read/write registers which are grouped by function and appear at different offsets within the memory space allocated to the card by the plug and play BIOS / operating system.

Note: For PCIe the 32-bit registers appear in the lower 32 bits of 64-bit locations and hence all byte offsets are multiplied by two.

Offset		Read Function	Write Function
PCI	PCIe		
00h	00h	Special Function status / control register SFS ₃₁ — 16 SFR ₁₅ 0	Special Function clear / control register SFC ₃₁ 16 SFR ₁₅ 0
04h	08h	Interrupt request / mask register IRR ₃₁ — 16 IMR ₁₅ 0	Interrupt mask register IMR ₁₅ 0
08h	10h	Timer counter / latch TMRC ₃₁ — 16 TMRL ₇₋₀	Timer latch TMRL ₇₋₀
0Ch	18h	Time Stamper counter / latch TSTC ₃₁ — 16 TSTL ₁₅ — 0	
10h	20h	Pulse Generator 0 counter / latch PG0C ₃₁ — 16 PG0L ₁₅ — 0	Pulse Generator 0 latch PG0L ₁₅ — 0
20h	40h	Digital I/O bus 0 mux / status DOM ₃₁ — 16 DIOS ₁₅ — 0	Digital I/O bus 0 mux / control DOM ₃₁ — 16 DOC ₇₋₀
24h	48h	Digital I/O bus 1 direction / status DIOD ₁₇₋₁₆ DIOS ₁₅ — 0	Digital I/O bus 1 control DIOC ₁₅ — 0
28h	50h	Digital I/O bus 2 direction / status DIOD ₁₇₋₁₆ DIOS ₁₅ — 0	Digital I/O bus 2 control DIOC ₁₅ — 0
40h	80h	X Channel status / control register CSR ₃₁ — 16 TSTL ₁₅ — 0	X Channel clear / control register CCLR ₃₁ — 16 CCR ₁₅ 0
44h	88h	Y Channel status / control register CSR ₃₁ — 16 TSTL ₁₅ — 0	Y Channel clear / control register CCLR ₃₁ — 16 CCR ₁₅ 0
48h	90h	Z Channel status / control register CSR ₃₁ — 16 TSTL ₁₅ — 0	Z Channel clear / control register CCLR ₃₁ — 16 CCR ₁₅ 0
	A0h	S Channel status / control CSR ₃₁ — 16 TSTL ₁₅ — 0	S Channel clear / control register CCLR ₃₁ — 16 CCR ₁₅ 0
60h	C0h	X Timer Latch D ₃₁ 0	X Timer Latch D ₃₁ 0
64h	C8h	Y Timer Latch D ₃₁ 0	Y Timer Latch D ₃₁ 0
68h	D0h	Z Timer Latch D ₃₁ 0	Z Timer Latch D ₃₁ 0

Offset		Read Function	Write Function
PCI	PCIe		
	E0h	S Timer Latch D31 0	S Timer Latch D31 0
80h	100h	X Marker latch D31 0	X Marker latch D31 0
84h	108h	Y Marker latch D31 0	Y Marker latch D31 0
88h	110h	Z Marker latch D31 0	Z Marker latch D31 0
	120h	S Marker latch D31 0	S Marker latch D31 0
A0h	140h	X Probe latch D31 0	X Probe latch D31 0
A4h	148h	Y Probe latch D31 0	Y Probe latch D31 0
A8h	150h	Z Probe latch D31 0	Z Probe latch D31 0
	160h	S Probe latch D31 0	S Probe latch D31 0

Special function control register – PCI 00h, PCIe 00h

The lower 16 bits of the register at offset 00h are designated the special function control register. This read/write register allows control of board-based facilities. The register contents are zero after system reset.

Special function control register:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UR0	PG0cr[3:0]				PG0ie	PG0e	DI0ie	TSTs[2:0]			TMRe	Fs	Be	Fe	Pe

Key:

Pe	Enable / Disable probe function
Fe	Enable / Disable footswitch function
Be	Enable / Disable buzzer output
Fs	Footswitch input sense
TMRe	Enable / Disable timer function
TSTs	Time stamper event select register
DI0ie	Enable / Disable board digital input 0 interrupt
PG0e	Enable / Disable pulse generator 0 function
PG0ie	Enable / Disable pulse generator 0 interrupt
PG0cr	Pulse generator 0 control register
UR0	Enable / Disable user request 0 flag

Time stamper event sources:

TSTs	Source
0	Probe occur flag
1	Timer Sync occur flag
2	User Request 0 flag
3	Board Digital Input 0 occur flag
4	Pulse Generator 0 Sync occur flag
5	Axis Compare 0 Sync occur flag
6	Axis Compare 1 Sync occur flag
7	Reserved

Pulse Generator 0 control register bit fields:

PG0cr bit	Function
0	Direction of operation (1=positive, 0=negative)
1	Bi-Directional mode (1=On, 0=Off)
2	Hardware Control Start/Stop (1=On, 0=Off)
3	Deglintch mode (1=On, 0=Off)

Special function clear register – PCI 00h, PCIe 00h

The upper 16 bits of the register at offset 00h are designated the Special function clear register. This write-only register can be used to clear occur flags of board-based facilities by writing '1' to the equivalent bit. The status of all relevant flags is cleared after system reset.

Special function clear register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	-	-	-	PG0c	DI0c	-	-	TSTc	TMRc	-	-	-	-

Key:

TMRc	Clear timer occur flag
TSTc	Clear time stamper overflow occur flag
DI0c	Clear board digital input 0 occur flag
PG0c	Clear pulse generator 0 occur flag

Special function status register – PCI 00h, PCIe 00h

The upper 16 bits of the register at offset 00h are designated the Special function status register. This read only register allows access to board-based status information.

Special function status register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	-	-	-	PG0o	DI0o	AC1o	AC0o	TSTo	TMRo	Fi	nPi	Fo	Po

Key:

Po	Probe occur flag
Fo	Footswitch occur flag
nPi	Direct probe input (inverted)
Fi	Direct footswitch input
TMRo	Timer occur flag
TSTo	Time Stamper overflow occur flag
AC0o	Axis Compare 0 occur flag
AC1o	Axis Compare 1 occur flag

DI0o Board Digital Input 0 occur flag

PG0o Pulse Generator 0 occur flag

Interrupt mask register – PCI 04h, PCIe 08h

This 16-bit read / write register sets the interrupt masks to select which interrupt sources generate interrupts. A logic 0 disables an interrupt and a logic 1 enables an interrupt. The register holds zero after system reset. The bit assignment for this register is as follows:

Interrupt mask register:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	CH3ie	CH2ie	CH1ie	CH0ie	-	-	-	-	-	-	BRDie	TMRie

Key:

Bit	Description	Source
TMRie	Timer interrupt enable	Timer (reload) occur flag
BRDie	Board interrupts enable	Board occur flags (Probe, Pulse Generator 0, Board Digital Input 0)
CH0ie	Channel 0 interrupts enable	Channel 0 occur flags (Marker, Zero, Channel Digital Input 0, Axis Compare 0/1)
CH1ie	Channel 1 interrupts enable	Channel 1 occur flags (Marker, Zero, Channel Digital Input 0)
CH2ie	Channel 2 interrupts enable	Channel 2 occur flags (Marker, Zero, Channel Digital Input 0)
CH3ie	Channel 2 interrupts enable	Channel 3 occur flags (Marker, Zero, Channel Digital Input 0)

Interrupt request register – PCI 04h, PCIe 08h

This 16-bit read-only register indicates which interrupt sources have generated interrupts. logic 1 indicates that an interrupt has occurred. To clear an interrupt request, the occurred flags of all associated interrupt sources must be cleared. The register holds 00h after system reset. Please note that since the PCI/PCIE interrupt system is level sensitive, all interrupt requests must be cleared to free the interrupt line allocated to the interface. The bit assignment for this register is as follows:

Interrupt request register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	-	CH3io	CH2io	CH1io	CH0io	-	-	-	-	-	-	BRDio	TMRio

Key:

TMRio Timer interrupt occurred

BRDio Board interrupt(s) occurred

CH0io Channel 0 interrupt(s) occurred

CH1io Channel 1 interrupt(s) occurred

CH2io Channel 2 interrupt(s) occurred

CH3io Channel 3 interrupt(s) occurred

Timer latch – PCI 08h, PCIe 10h

The lower 8 bits of the register at offset 08h are designated the Timer Latch. This read / write register specifies the reload value (in 0.1ms) of the Timer function. This register holds FFh after system reset.

Timer counter – PCI 08h, PCIe 10h

The upper 16 bits of the register at offset 08h are designated the Timer Counter. This read-only register returns the current value of the (count-down) timer counter (in 0.1ms). When the timer function is disabled, the timer counter resets to the value of the timer latch.

Time Stamper latch – PCI 0Ch, PCIe 18h

The lower 16 bits of the register at offset 0Ch are designated the Time Stamper Latch. This read-only register allows access to the timestamp of the event associated with the Time Stamper. The register holds zero after system reset.

Time Stamper counter – PCI 0Ch, PCIe 18h

The upper 16 bits of the register at offset 0Ch are designated the Time Stamper Counter. This read-only register returns the current value of the (count-up) time stamper counter (in 1 μ s).

Pulse Generator 0 latch – PCI 10h, PCIe 20h

The lower 16 bits of the register at offset 10h are designated the Pulse Generator 0 Latch. This read / write register specifies the reload value (in quadrature counts) of the pulse generator 0 function. Writing to this register resets the pulse generator 0 counter. This register holds zero after system reset.

Pulse Generator 0 counter – PCI 10h, PCIe 20h

The upper 16 bits of the register at offset 10h are designated the Pulse Generator 0 Counter. This read-only register returns the current value of the pulse generator 0 (up/down) counter (in quadrature counts). The pulse generator 0 counter resets to zero on a write operation to the pulse generator 0 latch. This register holds zero after system reset.

Digital I/O control / status register – PCI 20h, 24h, 28h, PCIe 40h,48h,50h

The lower 16 bits of these registers are designated the Digital I/O Control / Status Registers. These read / write registers allow control of the digital outputs and access to the digital inputs of the equivalent I/O bus. The register contents are zero after system reset.

Please note that on Digital I/O bus 0, I/Os 0 to 7 are hardwired as outputs and I/Os 8 to 15 are hardwired as inputs.

Digital I/O bus 0 mux register – PCI 20h, PCIe 40h

The upper 16 bits of this register are designated the Digital I/O Bus 0 Mux Register. This read / write register allows control of the multiplexers (source selectors) of digital outputs on I/O bus 0. For each digital output there are 2 selection bits, allowing for 4 possible signal sources. For a list of possible source routings on each pin, please refer to Section 4.1.4.1.

Digital I/O bus 0 mux register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
D07s[1:0]		D06s[1:0]		D05s[1:0]		D04s[1:0]		D03s[1:0]		D02s[1:0]		D01s[1:0]		D00s[1:0]	

Digital I/O direction register – PCI 24h, 28h, PCIe 48h,50h

The upper 16 bits of this register are designated the Digital I/O Direction Registers. These read / write registers control the direction of digital I/Os.

Digital I/O direction register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	IOb1d	IOb0d

Key:

IOb0d Direction of digital I/O byte 0 (1=Input, 0=Output)

IOb1d Direction of digital I/O byte 1 (1=Input, 0=Output)

Channel control register – PCI 40h, 44h, 48h, PCIe 80h,88h,90h,98h

The lower write-only 16 bits of these registers are designated the Channel Control Registers. These read / write registers allow control of channel-based facilities. The register contents are zero after system reset.

Channel control register:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L2s[2:0]			L1s[2:0]			L0s[1:0]		DI0ie	MSe	Ze	invZ	invM	invB	invA	Me

Key:

Me Enable / Disable marker function

invA Invert signal A

invB Invert signal B

invM Invert signal M

invZ Invert signal Z

Ze Enable / Disable zero function

MSe Enable / Disable marker synchronisation with signals A & B

DI0ie Enable / Disable channel digital input 0 interrupt

L0s Latch 0 (Timer latch) select register

L1s Latch 1 (Marker latch) select register

L2s Latch 2 (Probe latch) select register

Source events of Latch 0 (Timer latch):

L0s	Source
0	Timer Sync occur flag
1	Count (default)
2	Pulse Generator 0 Sync occur flag
3	User Request 0 flag

Source events of Latch 1 (Marker latch):

L1s	Source
0	Marker occur flag
1	Zero occur flag
2	Pulse Generator 0 Sync occur flag
3	User Request 0 flag
4	Channel Digital Input 0 occur flag
5	Axis Compare 0 Sync occur flag
6	Axis Compare 1 Sync occur flag
7	Count

Source events of Latch 2 (Probe latch):

L2s	Source
0	Probe occur flag
1	N/A (direct counter read)
2	Pulse Generator 0 Sync occur flag
3	User Request 0 flag
4	Channel Digital Input 0 occur flag
5	Axis Compare 0 Sync occur flag
6	Axis Compare 1 Sync occur flag
7	Count

Channel time Stamper latch – PCI 40h, 44h, 48h, PCIe 80h,88h,90h,98h

The lower read-only 16 bits of these registers are designated the Time Stamper Latch. This read-only register allows access to the timestamp of the event associated with the Time Stamper. The register holds zero after system reset.

Channel clear register and extended channel control register – PCI 40h, 44h, 48h, PCIe 80h,88h,90h,98h

The upper bits [31-24] of these registers are designated the Channel Clear Registers. These write-only registers can be used to clear occur flags of channel-based facilities by writing '1' to the equivalent bit. The status of all relevant flags is cleared after system reset. The upper bits [21-16] are designated the extended channel control registers and are write-only.

Channel clear and extended channel control registers:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	AC1c	AC0c	ER1c	ER0c	DI0c	-	-	CNTM[1:0]	CNTI	L3s[2:0]			

Key:

CNTI	Count inhibit
CNTM	Count Mode (see below)
DI0c	Clear channel digital input 0 occur flag
ER0c	Clear error 0 (quadrature) occur flag
ER1c	Clear error 1 (power) occur flag
AC0c	Clear axis compare 0 occur flag
AC1c	Clear axis compare 1 occur flag

Source events of Latch 3 (Time stamp latch):

L3s	Source
0	Count
1	Marker occur flag
2	Zero occur flag
3	Pulse Generator 0 Sync occur flag
4	User Request 0 flag
5	Channel Digital Input 0 occur flag
6	Axis Compare 0 Sync occur flag
7	Axis Compare 1 Sync occur flag

Count mode:

CNTM	Source
0	Quadrature AB decode
1	Count rising and falling edges of A, B selects count up/down direction
2	Count rising edges of A, B selects count up/down direction

Channel status register – PCI 40h, 44h, 48h, PCIe 80h,88h,90h,98h

The upper 16 bits of these registers are designated the Channel Status Registers. These read-only registers allow access to channel-based status information.

Channel status register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	AC1o	AC0o	ER1o	ER0o	DI0o	nLIM1	nLIM0	Zo	Zi	Mi	Bi	Ai	Mo

Key:

Mo	Marker occur flag
Ai	Direct A channel input
Bi	Direct B channel input
Mi	Direct M (marker) channel input
Zi	Direct Z (zero) channel input
Zo	Zero occur flag
nLIM0	Direct Limit 0 channel input (inverted)
nLIM1	Direct Limit 1 channel input (inverted)
DI0o	Channel digital input 0 occur flag
ER0o	Error 0 (quadrature) occur flag
ER1o	Error 1 (power) occur flag
AC0o	Axis compare 0 occur flag
AC1o	Axis compare 1 occur flag

Latch 0 (Timer latch) – PCI 60h, 64h, 68h, PCIe c0h,c8h,d0h,d8h

These three registers allow access to the three 32-bit Timer Latches. Each latch stores the counter value when the associated source event occurs and should only be read when the occur flag of that event is set. Various source events can be selected by the equivalent source event selector, accessible through the channel control register. The register contents are zero after system reset.

Latch 1 (Marker Latch) – PCI 80h,84h,88h, PCIe 100h,108h,110h,118h

These three registers allow access to the three 32-bit Marker Latches. Each latch stores the counter value when the associated source event occurs and should only be read when the occur flag of that event is set. Various source events can be selected by the equivalent source event selector, accessible through the channel control register. The register contents are zero after system reset.

Latch 2 (Probe Latch) – PCI a0h,a4h,a8h, PCIe 120h,128h,130h,138h

These three registers allow access to the three 32-bit Probe Latches. Each latch stores the counter value when the associated source event occurs and should only be read when the occur flag of that event is set. Various source events can be selected by the equivalent source event selector, accessible through the channel control register. The register contents are zero after system reset.

Appendix B - Absolute Card Register Reference

The Deva001 Absolute Encoder Interface card is supplied with a variety of device drivers for Microsoft Windows operating systems which perform all low-level access functions required for its operation. Using a device driver offers several benefits including the ability to re-use application software and routines with any of Deva Electronics compatible products. The device drivers and the common software interface are described in Section 1 and Section 2 of this manual. For applications where hardware access is essential, the following text gives an overview of the register set and card functionality.

Register address map

The card implements several 32-bit read/write registers grouped by function and appear at different offsets within the memory space allocated by the plug and play BIOS / operating system. For PCIe the 32-bit registers appear in the lower 32 bits of 64-bit locations and hence all byte offsets are multiplied by two.

Offset		Read Function	Write Function
PCI	PCIe		
00h	00h	Special Function status / control register	Special Function clear / control register
		SFS ₃₁ — 16 SFR ₁₅ 0	SFC ₃₁ 16 SFR ₁₅ 0
04h	08h	Interrupt request / mask register	Interrupt mask register
		IRR ₃₁ — 16 IMR ₁₅ 0	IMR ₁₅ 0
08h	10h	Timer counter / latch	Timer latch
		TMRC ₃₁ — 16 TMRL ₇ - 0	TMRL ₇ - 0
0Ch	18h	Time Stamper counter / latch	
		TSTC ₃₁ — 16 TSTL ₁₅ — 0	
10h	20h		
20h	40h	Digital Output bus 0 mux / I/O bus 0 status	Digital Output bus 0 mux / control
		DOM ₃₁ — 16 DIOS ₁₅ — 0	DOM ₃₁ — 16 DOC ₇ - 0
24h	48h	Digital I/O bus 1 direction / status	Digital I/O bus 1 control
		DIOD ₁₇ - 16 DIOS ₁₅ — 0	DIOC ₁₅ — 0
28h	50h	Digital I/O bus 2 direction / status	Digital I/O bus 2 control
		DIOD ₁₇ - 16 DIOS ₁₅ — 0	DIOC ₁₅ — 0
40h	80h	X Channel status / control register	X Channel clear / control register
		CSR ₃₁ — 16 CCR ₁₅ 0	CCR ₁₅ 0
44h	88h	Y Channel status / control register	Y Channel clear / control register
		CSR ₃₁ — 16 CCR ₁₅ 0	CCR ₁₅ 0
48h	90h	Z Channel status / control register	Z Channel clear / control register
		CSR ₃₁ — 16 CCR ₁₅ 0	CCR ₁₅ 0
	A0h	S Channel status / control register	S Channel clear / control register
		CSR ₃₁ — 16 CCR ₁₅ 0	CCR ₁₅ 0
60h	C0h	X Latch	
		D ₃₁ 0	
64h	C8h	Y Latch	
		D ₃₁ 0	

Offset		Read Function	Write Function
PCI	PCle		
68h	D0h	Z Latch	
		D31 0	
	D8h	S Latch	
		D31 0	
C0h	180h	X Channel control register 1	X Channel control register 1
		CCR15 0	CCR15 0
C4h	188h	Y Channel control register 1	Y Channel control register 1
		CCR15 0	CCR15 0
C8h	190h	Z Channel control register 1	Z Channel control register 1
		CCR15 0	CCR15 0
	198h	S Channel control register 1	S Channel control register 1
		CCR15 0	

Special Function Control Register – PCI 00h, PCle 00h

The lower 16 bits of the register at offset 00h are designated the Special Function Control Register. This read/write register allows control of board-based facilities. The register contents are zero after system reset.

Special Function Control Register:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UR0	-	-	-	-	-	-	DI0ie	TSTs[2:0]			TMRe	-		-	-

Key:

TMRe Enable / Disable timer function
TSTs Time stamper event select register
DI0ie Enable / Disable board digital input 0 interrupt
UR0 Enable / Disable user request 0 flag

Time stamper event sources:

TSTs	Source
1	Timer Sync occur flag
2	User Request 0 flag
3	Board Digital Input 0 occur flag
4	Pulse Generator 0 Sync occur flag

Special Function Clear Register – PCI 00h, PCle 00h

The upper 16 bits of the register at offset 00h are designated the Special Function Clear Register. This write-only register can be used to clear occur flags of board-based facilities by writing '1' to the equivalent bit. The status of all relevant flags is cleared after system reset.

Special Function Clear Register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	-	-	-	-	DI0c	-	-	TSTc	TMRc	-	-	-	-

Key:

TMRc Clear timer occur flag.

TSTc Clear time stamper overflow occur flag.

DI0c Clear board digital input 0 occur flag.

Special Function Status Register – PCI 00h, PCIe 00h

The upper 16 bits of the register at offset 00h are designated the Special Function Status Register. This read only register allows access to board-based status information. These bits are treated as 'don't cares' when writing to this offset.

Special Function Status Register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	-	-	-	-	DI0o	-	-	TSTo	TMRo	-	-	-	-

Key:

TMRo Timer occur flag

TSTo Time Stamper overflow occur flag

DI0o Board Digital Input 0 occur flag

Interrupt Mask Register – PCI 04h, PCIe 08h

This 16-bit read / write register sets the interrupt masks to select which interrupt sources generate interrupts. A logic 0 disables an interrupt and a logic 1 enables an interrupt. The register holds zero after system reset. The bit assignment for this register is as follows:

Interrupt Mask Register:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	CH3ie	CH2ie	CH1ie	CH0ie	-	-	-	-	-	-	BRDie	TMRie

Key:

TMRie Timer (reload) occur flag

BRDie Board occur flag

CH0ie Channel 0 occur flag

CH1ie Channel 1 occur flag

CH2ie Channel 2 occur flag

CH3ie Channel 3 occur flags

Interrupt Request Register – PCI 04h, PCIe 08h

This 16-bit read-only register indicates which interrupt sources have generated interrupts. Logic 1 indicates that an interrupt has occurred. To clear an interrupt request, the occurred flags of all associated interrupt sources must be cleared. The register holds 00h after system reset. Please note that since the PCI/PCIe interrupt system is level sensitive, all interrupt requests must be cleared to free the interrupt line allocated to the card. The bit assignment for this register is as follows:

Interrupt Request Register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	-	CH3io	CH2io	CH1io	CH0io	-	-	-	-	-	-	BRDio	TMRio

Key:

TMRio Timer interrupt occurred
 BRDio Board interrupt(s) occurred
 CH0io Channel 0 interrupt(s) occurred
 CH1io Channel 1 interrupt(s) occurred
 CH2io Channel 2 interrupt(s) occurred
 CH3io Channel 3 interrupt(s) occurred

Timer Latch – PCI 08h, PCIe 10h

The lower 8 bits of the register at offset 08h are designated the Timer Latch. This read / write register specifies the reload value (in 0.1ms) of the Timer function. This register holds FFh after system reset.

Timer Counter – PCI 08h, PCIe 10h

The upper 8 bits of the register at offset 08h are designated the Timer Counter. This read-only register returns the current value of the (count-down) timer counter (in 0.1ms). When the timer function is disabled, the timer counter resets to the value of the timer latch.

Time Stamper Latch – PCI 0Ch, PCIe 18h

The lower 16 bits of the register at offset 0Ch are designated the Time Stamper Latch. This read-only register allows access to the timestamp of the event associated with the Time Stamper. The register holds zero after system reset.

Time Stamper Counter – PCI 0Ch, PCIe 18h

The upper 16 bits of the register at offset 0Ch are designated the Time Stamper Counter. This read-only register returns the current value of the (count-up) time stamper counter (in 1µs).

Digital I/O Control / Status Register – PCI 20h, 24h, 28h, PCIe 40h,48h,50h

The lower 16 bits of these registers are designated the Digital I/O Control / Status Registers. These read / write registers allow control of the digital outputs and access to the digital inputs of the equivalent I/O bus. The register contents are zero after system reset.

Please note that on Digital I/O bus 0, I/Os 0 to 7 are hardwired as outputs and I/Os 8 to 15 are hardwired as inputs.

Digital I/O Bus 0 Mux Register – PCI 20h, PCIe 40h

The upper 16 bits of this register are designated the Digital I/O Bus 0 Mux Register. This read / write register allows control of the multiplexers (source selectors) of digital outputs on I/O bus 0. For each digital output there are 2 selection bits, allowing for 4 possible signal sources. For a list of possible source routings on each pin, please refer to Section 5.1.3.1.

Digital I/O Bus 0 Mux Register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
D07s[1:0]		D06s[1:0]		D05s[1:0]		D04s[1:0]		D03s[1:0]		D02s[1:0]		D01s[1:0]		D00s[1:0]	

Digital I/O Direction Register – PCI 24h, 28h, PCIe 48h,50h

The upper 16 bits of this register are designated the Digital I/O Direction Registers. These read / write registers control the direction of digital I/Os.

Digital I/O Direction Register:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	IOb1d	IOb0d

Key:

IOb0d Direction of digital I/O byte 0 (1=Input, 0=Output)

IOb1d Direction of digital I/O byte 1 (1=Input, 0=Output)

Channel Control Register 0– PCI 40h, 44h, 48h, PCIe 80h,88h,90h,98h

The lower 16 bits of these registers are designated Channel Control Register 0. These read / write registers are used to configure the data acquisition mode (such as clock frequency and bit length) from the SSI encoder. There is a register for each channel. The registers hold zero after a system reset.

Channel Control Register 0:

Bit 15	Bit 14	Bit 13 - Bit 12	Bit 11 - Bit 8	Bit 7 - Bit 3	Bit 2 - Bit 0
Out Output	Gray / Binary	Extra bit mode	Offset	Data length	Frequency
0 = Out Low 1 = Out High	0 = Binary mode 1 = Gray mode	0 = No Extra bit 1 = Power Fail bit 2 = Even Parity bit 3 = Odd Parity bit	0 to 15 bits	1 to 31 bits 0 = 32 bits	0 = 2.78 MHz 1 = 1.39 MHz 2 = 926 kHz 3 = 694 kHz 4 = 463 kHz 5 = 347 kHz 6 = 174 kHz 7 = 86.8 kHz

Channel Status Register 0 – PCI 40h, 44h, 48h, PCIe 80h,88h,90h,98h

The upper 16 bits of these registers are designated Channel Status Register 0. These read-only registers allow access to channel-based status information. These bits are treated as 'don't cares' when writing to these registers.

Channel Status Register 0:

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-	-	-	-	-	-	-	-	-	-	-	DI0o	RCo	RARF	PWRF	Di

Key:

Di	Direct SSI data channel input
PWRF	Power failure (or no encoder) flag
PARF	Parity failure flag
RCo	Read complete occur flag
DI0o	Channel digital input 0 occur flag

Channel Control Register 1 – PCI C0h,C4h,C8h, PCIe 180h,188h,190h,198h

The lower 16 bits of these registers are designated Channel Control Register 1. These read / write registers allow control of the SSI read trigger and other channel-based facilities. The registers hold zero after a system reset.

Channel Control Register 1:

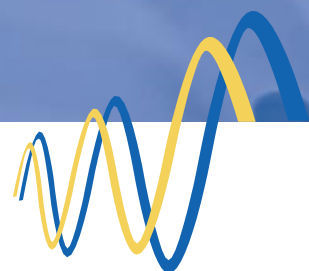
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	-	-	DI0ie	RCie	DI0e	RCe	RTs[2:0]		

Key:

RTs	Read trigger event select register
RCe	Enable / Disable read complete function
DI0e	Enable / Disable channel digital input 0 function
RCie	Enable / Disable read complete interrupt
DI0ie	Enable / Disable channel digital input 0 interrupt

Read trigger events:

RTs	Source
0	User Request 0 flag
1	Timer Sync occur flag
2	Channel Digital Input 0 occur flag
7	N/A (Continuous)



SUPPORT:

For additional downloadable Support Documentation, please visit
www.deva.co.uk/support-downloads

Or contact us at support@deva.co.uk